REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-129, 133, 134, 135, 139, 140, 143, and 150-174 remain active in this case, Claims 120, 133, 139 and 150 having been amended by way of the present Supplemental Amendment. In the Amendment filed Feb. 20, 2001, Claims 130-132, 136-138, 141-142 and 144-149 were canceled; Claims 120, 121, 123, 125, 127, 129, 133, 139, 143 and 150 amended, and Claims 151-174 added

The Amendment filed Feb. 20, 2001 was believed to be responsive to the Official Action of Nov. 20, 2000. In that amendment each ground for rejection and objection were addressed, and the remarks of that amendment are incorporated by reference herein.

In the outstanding Official Action, it was noted that the Amendment filed Feb. 20, 2001 "fails to completely address the indefiniteness rejections raised in said Office action of Paper No. 5," and indicated that the objected to terms, such as "program circuit," were themselves acceptable, but that "it is difficult to correlate into the specification to ascertain with a reasonable degree of certainty what is actually being claimed. See 37 CFR 1.111."

In response to the Examiner's statements in the outstanding Official Action, Claims 120, 133, 139 and 150 have been amended to re-state the previously stated language found to be clear, i.e., "program circuit," "read circuit," and "verify circuit," in view of the statement in the outstanding Official Action, that "[i]n fact, leaving out said word "program" makes the term even more indefinite." Additionally, in response to the statement that "it is difficult to correlate into the specification to ascertain with a reasonable degree of certainty what is

actually being claimed," Applicants identify the following structure disclosed in the specification as corresponding to the objected to limitations:

(1) The "program circuit" in claim 120 corresponds to the circuits of reference numerals 2, 7, 9, 10 and 11 of Fig. 1. The bit line control circuit 2 is described in Fig. 3.

(2) The "first bit line bias circuit" in claim 129 corresponds to Qn3, Qn4, Qn5, Qn6, Qn9, Qn10, Qn11, and Qn12 in Fig. 3.

(3) The "second bit line bias circuit" in claim 129 corresponds to Qn1 in Fig. 3.

(4) The "read circuit" in claim 133 corresponds to the circuits of reference numerals 2, 7, 9, 10 and 11 of Fig. 1.

(5) The "verify circuit" in claim 139 corresponds to the circuits of reference numerals 2, 7, 9, 10 and 11 of Fig. 1.

(6) The "bit line precharge circuit" in claim 143 correspond to Qn1 of Fig. 3.

(7) The "verify circuit" in claim 150 corresponds to the circuits of reference numerals 2, 7, 9, 10 and 11 of Fig. 1.

Accordingly, Applicants have acted in good faith to understand and respond to the indefiniteness rejection and have clearly correlated the claim terms with the structure disclosed in the specification whereby the Examiner can ascertain with a reasonable degree of certainty what structure disclosed in the specification corresponds to these claim limitations. It is therefore believed that Applicants are fully responsive to the issues raised in the Official Actions of Nov. 20, 2000 and April 30, 2001.

Consequently, in light of the present amendment and the Amendment filed Feb. 20, 2001, no further issues are believed to be outstanding, and the present application is believed

to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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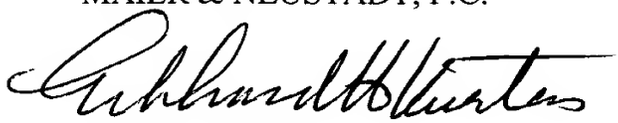

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Please amend Claims 120, 133, 139 and 150 as follows:

120. (Twice Amended) A multilevel nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a program circuit, coupled to said word lines and said bit line, for applying a write voltage to the word line of a selected memory cell, for applying a verify voltage to the word line of the selected memory cell to determine an actual threshold voltage of the selected memory cell while applying a pass voltage to remaining word lines of unselected memory fells in said NAND-cell unit to make the unselected memory cells act as transfer transistors, for applying a first level voltage to the bit line to change the threshold voltage of the selected memory cell in which it has been determined that the threshold voltage has not reached a given threshold voltage level, said first level voltage being combined with said write voltage, and for applying a second level voltage to the bit line to maintain the threshold voltage of the

selected memory cell in which it has been determined that the threshold voltage has reached said given threshold voltage level, said second level voltage being combined with said write voltage;

wherein said pass voltage is higher than said verify voltage.

133. (Twice Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a read circuit, coupled to said word lines and said bit line, for applying one of at least two read voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell is higher than said one of at least two read voltages while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two read voltages.

139. (Twice Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a verify circuit, coupled to said word lines and said bit line, for applying one of at least two verify voltages to the word line of a selected memory cell to determine whether or not a threshold voltage of the selected memory cell reaches one of said at least three threshold voltage levels while applying a pass voltage to remaining word lines of unselected memory cells in said NAND-cell unit to make the unselected memory cells act as transfer transistors;

wherein said pass voltage is higher than said at least two verify voltages.

150. (Twice Amended) A multi-level nonvolatile semiconductor memory device comprising:

a NAND-cell; unit including a plurality of memory cells connected in series, each of said memory cells including a transistor with a control gate and a charge storage portion and having storage states of at least three threshold voltage levels;

a plurality of word lines connected to respective control gates;

a bit line coupled to one end of said NAND-cell unit;

a verify circuit, coupled to said word lines and said bit line, for applying, to the word line of a selected memory cell, a first voltage in a first portion of a verify operation and a second voltage in second portion of said verify operation while applying, to remaining word lines of unselected memory cells in said NAND-cell unit, a third voltage in said first and second portions of said verify operation.